IN THE CLAIMS

The claims are not amended, but are reproduced here for the Examiner's convenience.

1. (Original) A method of preparing a circuit model for simulation comprising:

decomposing the circuit model having a number of latches into a plurality of extended latch boundary components; and

partitioning the plurality of extended latch boundary components.

2. (Original) The method of claim 1, wherein decomposing a circuit model having a number of latches into a plurality of extended latch boundary components comprises:

decomposing at least one of a plurality of hierarchical cells into one of the plurality of extended latch boundary components.

3. (Original) The method of claim 2, wherein partitioning the plurality of extended latch boundary components comprises:

using a constructive bin-packing heuristic to partition the plurality of extended latch boundary components.

4. (Original) The method of claim 3, wherein using a constructive bin-packing heuristic to partition the plurality of extended latch boundary components comprises:

constructing a plurality of seeds from the plurality of extended latch boundary components; and

merging the plurality of extended latch boundary components with the plurality of seeds.

5. (Original) The method of claim 1, wherein decomposing a circuit model having a number of latches into a plurality of extend latch boundary components comprises:

identifying an extended latch boundary component that meets a size constraint for at least one of a plurality of hierarchical cells.

6. (Original) The method of claim 5, wherein partitioning the plurality of extended latch boundary components comprises:

grouping the plurality of extended latch boundary components into a plurality of partitions by approximately equalizing the number of latches in each of the plurality of partitions.

7. (Original) The method of claim 1, wherein partitioning the plurality of extended latch boundary components comprises:

grouping the plurality of extended latch boundary components to form a plurality of partitions, each of the plurality of partitions having a size.

8. (Original) The method of claim 7, wherein partitioning the plurality of extended latch boundary components comprises:

partitioning the plurality of extended latch boundary components by approximately equalizing the number of latches in each of the plurality of partitions, approximately equalizing the latches that are activated in each of the plurality of partitions, and approximately equalizing the size of each of the plurality of partitions.

9. (Original) The method of claim 1, wherein partitioning the plurality of extended latch boundary components comprises:

attempting to partition the plurality of extended latch boundary components based on activity load balancing.

10. (Original) A method of preparing a circuit model for simulation, the circuit model having a model size, and the method comprising:

merging a plurality of extended latch boundary components into a plurality of partitions having a partition size; and

maintaining a load balance within the plurality of partitions.

11. (Original) The method of claim 10, further comprising:

reducing circuit overlap within the plurality of partitions.

12. (Original) The method of claim 11, further comprising:

adjusting the load balance to obtain a partition size of less than about 110% of the model size.

13. (Original) The method of claim 12, further comprising:

adjusting the load balance to obtain a partition size of less than about 120% of the model size.

14. (Original) A method of preparing a circuit model for a simulation having a total simulation time, the method comprising:

grouping a plurality of extended latch boundary components into a plurality of partitions; and

reducing the communication time within the plurality of partitions by adjusting the grouping.

15. (Original) The method of claim 14, further comprising:

reducing the communication time within the plurality of partitions to less than about ten percent of the total simulation time by adjusting the grouping.

16. (Original) A method of forming an extended latch boundary component comprising:

selecting a path having a first node selected from a group consisting of latches and primary outputs and a second node selected from a group consisting of latches and primary inputs, wherein the path can include a latch between the first node and the second node.

17. (Original) A latch boundary component comprising:

a path comprising a plurality of first nodes selected from a group consisting of latches and primary outputs and a plurality of second nodes selected from a group consisting of latches and primary inputs, where the path can include a plurality of latches between the plurality of first nodes and the plurality of second nodes.

18. (Original) A method of sharing a repeated circuit structure in a circuit model, the method comprising:

expanding the repeated circuit structure once to form an expanded circuit structure; and

grafting the expanded circuit structure to the circuit model as needed.

19. (Original) The method of claim 18, wherein grafting the expanded circuit structure to the circuit model as needed comprises:

copying a table representing the expanded circuit structure into the circuit model.

20. (Original) The method of claim 18, wherein grafting the expanded circuit structure to the circuit model as needed comprises:

altering a table representing the circuit model to add the expanded circuit structure.

21. (Original) A method of simulating a circuit model, the method comprising:

partitioning a plurality of extended latch boundary components to form a plurality of partitions having a size;

preparing a plurality of simulations from the plurality of partitions; and

executing the plurality of simulations on a processing unit.

22. (Original) The method of claim 21, further comprising:

adjusting the size of the plurality of partitions.

23. (Original) The method of claim 22, wherein executing the plurality of simulations on a processing unit comprises:

executing the plurality of simulations on a plurality of distributed processors.

24. (Original) A computer system comprising:

a processor unit;

a dicing unit operably coupled to the processor unit, capable of executing on the processor unit, and capable of decomposing a circuit model into a plurality of extended latch boundary components, and capable of partitioning the plurality of extended latch boundary components; and

a simulation unit operably coupled to the dicing unit and the processor unit, and capable of executing on the processor unit.

25. (Original) The computer system of claim 24, wherein the processor unit is a plurality of distributed processor units.

26. (Original) The computer system of claim 25, wherein the dicing unit is capable of load balancing.

27. (Original) The computer system of claim 26, wherein the dicing unit is capable of activity load balancing.

28. (Previously Presented) A computer-readable medium having computer-executable instructions, wherein the computer-executable instructions, when accessed, result in a machine performing:

partitioning a circuit model into a plurality of cells arranged in a hierarchy; and

mapping a plurality of extended latch boundary components into the circuit model by finding each cell in the plurality of cells that is highest in the hierarchy such that a single extended latch boundary component satisfying a given size constraint can be mapped into the cell.